AF/2813

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Guoqiang Xing, et al.	Docket No:	TI-31729
Serial No:	09/901,416	Conf. No:	7364
Examiner:	Thanh T. Nguyen	Art Unit:	2813
Filed:	07/09/2001		
For:	DUAL HARDMASK PROCESS FOR THE FORMATION OF COPPER/LOW-K INTERCONNECTS		

APPEAL BRIEF UNDER 37 C.F.R. 1.192

Mail Stop Appeal Brief - Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed March 23, 2003, and the Advisory Action mailed June 9, 2003.

Real Party in Interest under 37 C.F.R. 1.192(c)(1)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. 1.192 (c)(2)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the board's decision in the pending appeal.

Status of Claims on Appeal under 37 C.F.R. 1.192 (c)(3)

Claims 1-13 are rejected. Claims 1-13 are appealed.

Status of Amendments Filed After Final rejection under 37 C.F.R. 1.192 (c)(4)

No amendments were filed after final rejection under 37 C.F.R. 1.192(c)(4).

Summary of the Invention under 37 C.F.R. 1.192(c)(5)

The instant invention describes a dual hardmask process for the formation of Copper / Low-K interconnects. As shown in Figure 1(A), a copper layer 20 is formed in a dielectric layer 10. An etch stop layer 30 is formed over the copper layer 20 and dielectric layer 10, and a dielectric layer 40 is formed over the etch stop layer 30. A first hardmask layer 50 is formed over the dielectric layer 40 and a second hardmask layer 60 is formed over the first hardmask layer 50. A patterned photoresist layer 80 is formed over the second hardmask layer 60 and the second hardmask layer is etched to define an opening (page 8, lines 11-21). The remaining structure following the stripping of the patterned photoresist layer 80 is shown in Figure 1(b). A second patterned photoresist layer 85 is formed over the structure of Figure 1(b) and an opening for a trench is formed in the first hardmask layer 50 as shown in Figure 1(c). At this point the trench can be etched or alternatively the photoresist can be removed and the trench etched using hardmask layer 50 as the etch mask (page 9, lines 21-24). The exposed first hardmask layer 50 is then selectively removed using the second hardmask layer 60 as the masking layer. The dielectric layer 40 is then etched using the second hardmask layer 60 as the etch mask as shown in Figure 1(e).

In an alternative embodiment, an etch stop layer 110 is formed between the dielectric layers 42 and 44. The hardmask layers are formed on the dielectric layer 44 and an opening is formed in the first hardmask layer 50 as shown in Figure 2(b). Using the patterned photoresist layer 85, an opening is formed in the first hardmask layer 50 as shown in figure 2(c). The dielectric layer 44 is then etched to the etch stop layer 110 as shown in Figure 2(d). Using the second hardmask layer 60 as a etch mask, the exposed portion of the first hardmask layer 50 and the exposed portion of the etch stop layer 110 is removed as shown in Figure 2(e) (page 14, lines 17-20). Using the

hardmask layer 60 as an etch mask, the exposed region of the dielectric layer 42 is then etched as shown in Figure 2(f).

Statement of Issues Presented for Review under 37 C.F.R. 1.192 (C)(6)

Are claims 1-13 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Flanner et al. (U.S. Patent No. 6, 410, 437) in view of Blosse et al. (U.S. Patent No. 6,399,512)?

Statement of the Grouping of Claims under 37 C.F.R. 1.192(C)(7)

Claims 1-13 stand or fall together.

Arguments

Are claims 1-13 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Flanner et al. (U.S. Patent No. 6, 410, 437) in view of Blosse et al. (U.S. Patent No. 6,399,512)?

Appellant contends that claims 1-13 are not properly rejected under 35 U.S.C. 103(a) as being unpatentable over Flanner et al. (U.S. Patent No. 6, 410, 437) in view of Blosse et al. (U.S. Patent No. 6,399,512).

In forming the rejection of the claims of the instant invention the examiner argues that layers 4 and 6 as shown in Figures 3-14 of the Flanner et al. patent (herein after Flanner) are hardmask layers. In particular, in an office action dated 3/24/03, the examiner states that Flanner teaches layer 4 uses as a mask layer to etch layer 6 (see Figure 5), and layer 6 uses as a mask layer to etch layers 8-14 (see Figure 6).

Hardmask is a term of art in semiconductor manufacturing and describes a layer that is used as a masking layer during an etching or similar process. Appellant would like to direct the board to Figures 3-6 of the Flanner et al patent where the photoresist mask 2 is shown. As shown in Figure 4, the photoresist layer 2 is patterned and used as a mask during the etching of the layer 4. Careful observation of Figure 5 shows the

presence of the photoresist layer 2 during the etching of layer 6. Clearly the photoresist layer 2 prevents the etching of the underlying layers 4 and 5 and is the masking layer during the etch process. Both the unetched regions of the layers 4 and 6 are covered and masked by the photoresist layer 2 during the etching process. The layer 6 does not act as a mask layer as incorrectly stated by the examiner. Layer 6 is merely part of a stack of layers that is etched using the photoresist layer 2 as an etch mask. Observation of Figure 6 further shows the presence of the photoresist layer during the etching of the underlying layers 8, 10, and 12. Clearly the photoresist layer 2 is still being used as the masking layer. Therefore it is the photoresist layer 2 that is used in Flanner as the mask and not the layers 4 and 6 as stated by the examiner. Examination of Figures 1(d), 1(e), 2(d), 2(e), and 2(f) of the instant disclosure clearly show that layers 50 and 60 both serve as etch masks during certain etch steps and both layers function as a hardmask layers. The photoresist layer is not present during these etch process. This feature of the instant invention is not described or taught in either Flanner or the Blosse et al. patent and claims 1-13 cannot be properly rejected under 103(a) as being unpatentable over the Flanner et al patent in view of the Blosse et al. patent. The claims 1-13 are allowable over the cited art.

In responding to the above the examiner stated in an action dated 6/09/2003 that , "[S]ince comprises claims leave the claims open for inclusion of addition process steps and conditions in the claimed methods, even between the enumerated process steps, which do not interfere with the order of the process steps as set forth in the claimed invention, hence the presence of the photoresist layer 2 formed over the hardmask layers 4 and 6 during the etch process in Flanner's teaching does not prevent or exclude the masking function of the hardmask layers 4 and 6 during the etching process to form a trench in the second dielectric layer." The examiner is correct in stating that the use of the term comprises allows for the inclusion of addition process steps. The examiner is however incorrect in the application of this tenet of patent law to layers 4 and 6. Layers 4 and 6 are not hardmask layers. They serve no masking function as that term is used in the instant invention. The use of the term "comprises" does not allow one to change the described function of an element of a prior art invention to another

function not described or taught in that reference. The examiners above described argument for rejecting claims 1-13 over Flanner is flawed and invalid and claims 1-13 are allowable over the cited art.

Conclusion

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-13 under 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,

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APPENDIX

Claims on Appeal

1. A method for forming interconnects, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first dielectric layer over said silicon substrate;

forming a second dielectric layer over said first dielectric layer wherein the dielectric constant of the second dielectric layer is less than 3.0;

forming a first hardmask layer over said second dielectric layer;

forming a second hardmask layer on said first hardmask layer wherein said second hardmask layer comprises a material selected from the group consisting of titanium aluminide (TiAl), titanium aluminum nitride (TiAlN), titanium nitride (TiN), aluminum nitride (AlN), tantalum aluminide (TaAl), and tantalum aluminum nitride (TaAlN);

forming a trench in said second dielectric; and

filling said trench with a conducting material.

2. The method of claim 1 wherein said second dielectric layer is OSG.

3. The method of claim 1 wherein said conducting material is copper.

4. The method of claim 1 wherein the material used to form the first hardmask layer is selected from the group consisting of silicon carbide and silicon nitride.

5. A method for forming interconnects, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first dielectric layer over said silicon substrate;

forming a second dielectric layer over said first dielectric layer wherein the dielectric constant of the second dielectric layer is less than 3.0;

forming a first hardmask layer over said second dielectric layer;

forming a second hardmask layer on said first hardmask layer wherein said second hardmask layer comprises a material selected from the group consisting of titanium aluminide (TiAl), titanium aluminum nitride (TiAlN), titanium nitride (TiN), aluminum nitride (AlN), tantalum aluminide (TaAl), and tantalum aluminum nitride (TaAlN);

etching a first opening in said second hardmask layer of a first width;

forming a first trench of a second width in said second dielectric layer wherein said second width is less than said first width;

etching a second opening in said first hardmask layer of a first width;

forming a second trench of a first width in said second dielectric layer wherein said second trench is positioned over said first trench; and

filling said first and second trenches with a conducting material.

6. The method of claim 5 wherein said second dielectric layer is OSG.

7. The method of claim 5 wherein said conducting material is copper.

8. The method of claim 5 wherein said first hardmask is a material selected from the group consisting of silicon nitride and silicon carbide.

9. A method for forming interconnects, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first etch stop layer over said silicon substrate;

forming a first dielectric layer over said first etch stop layer wherein the dielectric constant of the first dielectric layer is less than 3.0;

forming a second etch stop layer over said first dielectric layer;

forming a second dielectric layer over said second etch stop layer wherein the dielectric constant of the second dielectric layer is less than 3.0;

forming a first hardmask layer over said second dielectric layer;

forming a second hardmask layer on said first hardmask layer wherein said second hardmask layer comprises a material selected from the group consisting of titanium aluminide (TiAl), titanium aluminum nitride (TiAlN), titanium nitride (TiN), aluminum nitride (AlN), tantalum aluminide (TaAl), and tantalum aluminum nitride (TaAlN);

etching a first opening in said second hardmask layer of a first width;

forming a first trench of a second width in said second dielectric layer wherein said second width is less than said first width;

etching a second opening in said first hardmask layer of a first width;

forming a second trench of a first width in said second dielectric layer wherein said second trench is positioned over said first trench;

simultaneously etching said second trench to a depth of said second etch stop layer and said first trench to a depth of said first etch stop layer; and

filling said first and second trenches with a conducting material.

10. The method of claim 9 wherein said first dielectric layer is OSG.

11. The method of claim 9 wherein said second dielectric layer is OSG.

12. The method of claim 9 wherein said conducting material is copper.

13. The method of claim 9 wherein said first hardmask is a material selected from the group consisting of silicon nitride and silicon carbide.